Advantages of EABs in FLEX 10K Devices

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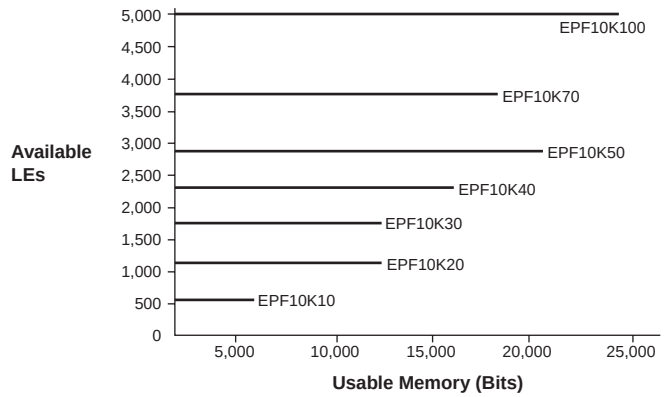
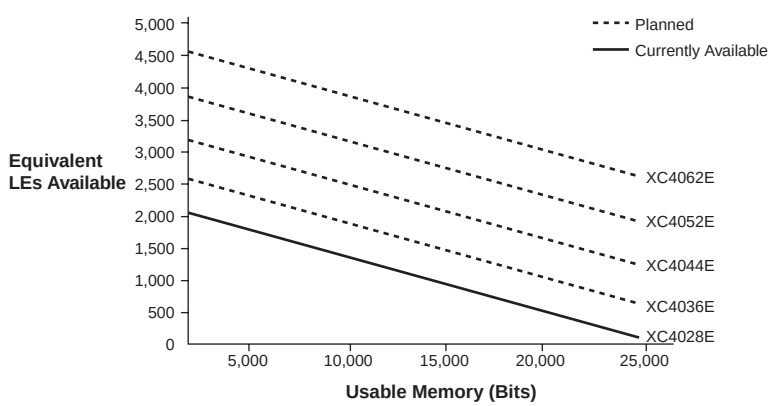
FLEX 10K devices contain both an embedded array and a logic array. The embedded array consists of a series of embedded array blocks (EABs), each containing 2,048 bits of RAM. Embedded array RAM offers better silicon efficiency, no impact on available logic, and higher performance than distributed RAM. The FLEX 10K architecture permits designers to simultaneously use the embedded array and the logic array. Figure 1 shows the logic and memory available in FLEX 10K devices.

Figure 1. Logic Elements (LEs) & On-Chip RAM Bits in FLEX 10K Devices



FPGAs with distributed RAM do not contain an embedded array. These devices typically have configurable logic blocks (CLBs) that can be configured as either logic or a small (e.g., 32×1 or 16×2) memory element. While distributed RAM is useful for small blocks of on-chip RAM, complex designs often require large blocks of RAM. With distributed RAM, the designer must trade logic for memory. Figure 2 demonstrates this tradeoff.

Figure 2. Xilinx XC4000 Logic & On-Chip RAM Tradeoff



Source: Xilinx XC4000 Series FPGA Product Specification v1.00

Performance

In FPGAs with distributed RAM, performance is dependent on the size of the memory and the number of routing resources used to construct the memory. To create large blocks of on-chip RAM, many small RAM blocks must be linked together, resulting in slow performance. In contrast, the performance of embedded array RAM is not affected by these factors; each EAB contains all the address decoding and synchronization circuitry required for consistent, optimal performance. Table 1 compares the performance of the FLEX 10K family and the Xilinx XC4000E family.

Table 1. On-Chip RAM Performance Comparison

Design	Xilinx XC4000E -3 Speed Grade	Xilinx XC4000E -2 Speed Grade *Note (1)*	Altera FLEX 10K -4 Speed Grade *Note (2)*	Altera FLEX 10K -3 Speed Grade *Note (2)*
Registered inputs & outputs for 256 X 8 on-chip RAM	63 Mhz	80 Mhz	86 Mhz	105 MHz

Notes:
(1) Source: Xilinx XC4000 Series FPGA Product Specification v1.00.
(2) Source: Altera ***1996 Data Book***.

Utilization

The FLEX 10K EAB architecture permits designers to use 100% of the available RAM bits as well as all the available LEs for logic. In contrast, creating large RAM blocks in distributed RAM FPGAs requires logic (CLBs) to multiplex the outputs of small RAM blocks and to control writing to the RAM. Moreover, CLBs that are used for logic cannot be used as RAM, so the logic capacity of a distributed RAM device decreases significantly as on-chip RAM is used. Designers should be forewarned that the maximum on-chip RAM claimed for some FPGAs may assume that all CLBs are configured as RAM. This assumption is misleading because some logic is required to combine the RAM into a large usable block.

Silicon Overhead

Synchronous RAM is typically easier to use than asynchronous RAM, but requires synchronization circuitry. The FLEX 10K architecture requires only a single synchronization circuit per EAB. For example, the 100,000-gate EPF10K100 has 12 EABs, and therefore requires 12 synchronization circuits (see Table 2).

Table 2. Required Synchronization Circuits for the FLEX 10K Family

	EPF10K10	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70	EPF10K100
Synchronization circuits *Note (1)*	3	6	6	8	10	9	12

Note:
(1) Source: Altera ***1996 Data Book***.

A distributed RAM architecture requires more synchronization circuitry compared with the Altera FLEX 10K architecture. For example, the Xilinx XC4000EX distributed RAM requires two synchronization circuits per CLB because each CLB is a discrete memory block, e.g., the 62,000-gate XC4062EX has 2,304 CLBs and requiring 4,608 RAM synchronization circuits (see Table 3). Even if the designer uses the CLB as logic, the overhead of on-chip RAM synchronization circuitry is present. This overhead increase die size and cost.

Table 3. Required Synchronization Circuits for the XC4000EX Family

	XC4028EX	XC4036EX	XC4044EX	XC4052EX	XC4062EX
Synchronization circuits *Note (1)*	2,048	2,592	3,200	3,872	4,608

Note:
(1) Source: Xilinx XC4000 Series FPGA Product Specification v1.00.

The documents listed below provide more detailed information. Part numbers are in parentheses.

Product Information Bulletins

PIB 20 *Benefits of Embedded RAM in FLEX 10K Devices (A-PIB-020-01)*
PIB 21 *Implementing Logic with Embedded Arrays in FLEX 10K Devices (A-PIB-021-01)*

Application Notes

AN 53 *Implementing Multipliers in FLEX 10K Devices (A-AN-053-01)*
AN 52 *RAM Functions in FLEX 10K Devices (A-AN-052-01)*

You can request these documents from:

- Altera Express fax service at (800) 5-ALTERA
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